REMARKS/ARGUMENTS

Claims 1-22 are pending.

Claims 1-16 are allowed. Claims 18-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jinno (US 2002/0167472) in view of Chung et al. (US 2004/0051685).

Applicant respectfully submits that all of the claims currently pending in this application are patentably distinguishable over the cited references for the following reasons, and reconsideration and allowance of this application are respectfully requested.

Independent claim 17 includes, among other limitations, "a transistor having a main electrode coupled to a voltage source," and "a first capacitor for charging a first voltage corresponding to a threshold voltage of the transistor." None of the cited references, alone or in combination, teach or suggest the above limitations.

Applicant respectfully submits that there is no motivation to combine Jinno and Chung references in a manner to meet the claim requirement. First, the two references are individually complete. In Jinno's FIG. 1, "a voltage value of the data voltage signal is held in the storage capacitor C. The conducting state (resistance) between the source (S) and the drain (D) of the second transistor Tr2 is controlled by the amount of charge held in the storage capacitor C. Further, the OEL element is driven by the current value which is determined by the power source voltage PVdd and the controlled resistance. More specifically, the resistance value of the second transistor Tr2, and thus the current value applied to the OEL, is controlled by the data voltage signal input to the first transistor Tr1." (Paragraph [0007], underlining added.).

Therefore, the capacitor C is used to control the resistance between the source (S) and the drain (D) of the second transistor Tr2 and has nothing to do with the threshold voltage of the transistor Tr2.

Similarly, Chung discloses a threshold voltage compensation circuit block between a data line and the pixels One threshold voltage compensation circuit block is connected commonly to a plurality of pixels, rather than be connected to every pixel. (See abstract). Therefore, the display device of Chung does not need a capacitor for each of its pixels. As a result, each of the Jinno and Chung references is complete and functional in itself, thus, there would be no reason to use or add parts to any of them.

Second, those skilled in the art of wafer processing would find it impractical to add the threshold voltage compensation circuit block of Chung to each pixel of Jinno.

The cited text of Jinno (FIG. 1) discloses a circuit for one pixel of a conventional active matrix display device. As shown, a capacitor (C1) is connected between the gate of transistor Tr2 and a fixed (supply) voltage of Vsc. The source of the transistor Tr2 is connected to a power source PVdd. A threshold voltage of the transistor Tr2 is the voltage between its gate terminal G and its source terminal (PVdd), that is, the voltage between the top terminal of the capacitor C1 and the power source PVdd. The voltage across the capacitor C1 can NOT be the same as the above-mentioned gate/source voltage of the transistor Tr2, unless Vsc is equal to PVdd. This is not the case in FIG. 1 of Jinno.

Accordingly, there is no motivation to combine Jinno and Chung references and thus independent claim 17 is also patentable over the cited references.

In view of the foregoing remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

47,947

By _____ For
Raymond R. Tabandeh
Reg. No. 43,945
626/795-9900